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10EC45

Fourth Semester B.E. Degree Examination, June/July 2013

Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Describe VHDL scalar data types with an example. **(08 Marks)**

b. Explain shift and rotate operators in HDL with an example. **(08 Marks)**

c. Write a note on simulation and synthesis. **(04 Marks)**

2 a. Explain the execution of signal assignment statements in HDL. **(05 Marks)**

b. Briefly discuss:

i) Constant declaration and assignment statement.

ii) Signal declaration and assignment statement. **(06 Marks)**

c. Write VHDL/Verilog code for 2 × 2 bit combinational array multiplier. **(09 Marks)**

3 a. Write VHDL code for 3 bit binary counter using CASE statement. **(06 Marks)**

b. Explain verilog casex. Write verilog description of priority encoder using casex statement. **(06 Marks)**

c. With syntax, explain the sequential statements in HDL:

i) IF statement ii) IF as ELSE-IF iii) For loop **(08 Marks)**

4 a. Write structural description of an VHDL SR latch using NOR gates. **(08 Marks)**

b. Write the facts of structural description. **(04 Marks)**

c. Write verilog code for N bit magnitude comparator using generate statement. **(08 Marks)**

PART – B

5 a. Write VHDL code to convert unsigned binary vector to integer conversion using procedure. **(08 Marks)**

b. Explain the syntax of function in verilog with an example. **(04 Marks)**

c. Write VHDL code for reading a string of characters from file and store in an array Ex: COLLEGE. **(08 Marks)**

6 a. Write VHDL code for 16 × 8 SRAM using mixed type description. **(12 Marks)**

b. Write verilog code for ALU using mixed type description. **(08 Marks)**

7 a. Write mixed language description of Master Slave D flip-flop by invoking VHDL entity from verilog module. **(10 Marks)**

b. Explain the process of invoking a verilog module from VHDL module. **(10 Marks)**

8 a. With an example, explain mapping the function statement in HDL. **(06 Marks)**

b. Discuss some important facts related to synthesis basics. **(06 Marks)**

c. With an example, explain mapping if, if-else, case statement in HDL. Show the synthesized logic symbol and gate level diagram. **(08 Marks)**

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